GTL2107

12-bit GTL–/GTL/GTL+ to LVTTL translator

Rev. 04 — 6 July 2007 | Product data sheet

1. General description

The GTL2107 is a customized translator between dual Xeon processors, GTL–/GTL/GTL+ I/O and the Platform Health Management, South Bridge and Power Supply 3.3 V LVTTL and GTL signals.

2. Features

- Operates as a GTL to LVTTL sampling receiver or LVTTL to GTL driver
- Operates at GTL, GTL+ or GTL– levels
- EN1 and EN2 enable control
- 3.0 V to 3.6 V operation
- LVTTL I/O not 5 V tolerant
- Series termination on the LVTTL outputs of 30 Ω
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 Class II, Level A which exceeds 500 mA
- Package offered: TSSOP28

3. Quick reference data

Table 1. Quick reference data

T_{amb} = 25 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{io}	input/output capacitance	A port; V_O = 3.0 V or 0 V	-	3.0	4.0	pF
		B port; V_O = V_{TT} or 0 V	-	2.0	3.0	pF
V_{ref} = 0.73 V; V_{TT} = 1.1 V						
t_{PLH}	LOW-to-HIGH propagation delay	nA to nBI; see Figure 4	1	4	8	ns
		nBI to nA or nAO (open-drain outputs); see Figure 14	2	13	18	ns
t_{PHL}	HIGH-to-LOW propagation delay	nA to nBI; see Figure 4	2	5.5	10	ns
		nBI to nA or nAO (open-drain outputs); see Figure 14	2	4	10	ns
V_{ref} = 0.76 V; V_{TT} = 1.2 V						
t_{PLH}	LOW-to-HIGH propagation delay	nA to nBI; see Figure 4	1	4	8	ns
		nBI to nA or nAO (open-drain outputs); see Figure 14	2	13	18	ns
t_{PHL}	HIGH-to-LOW propagation delay	nA to nBI; see Figure 4	2	5.5	10	ns
		nBI to nA or nAO (open-drain outputs); see Figure 14	2	4	10	ns

founded by Philips

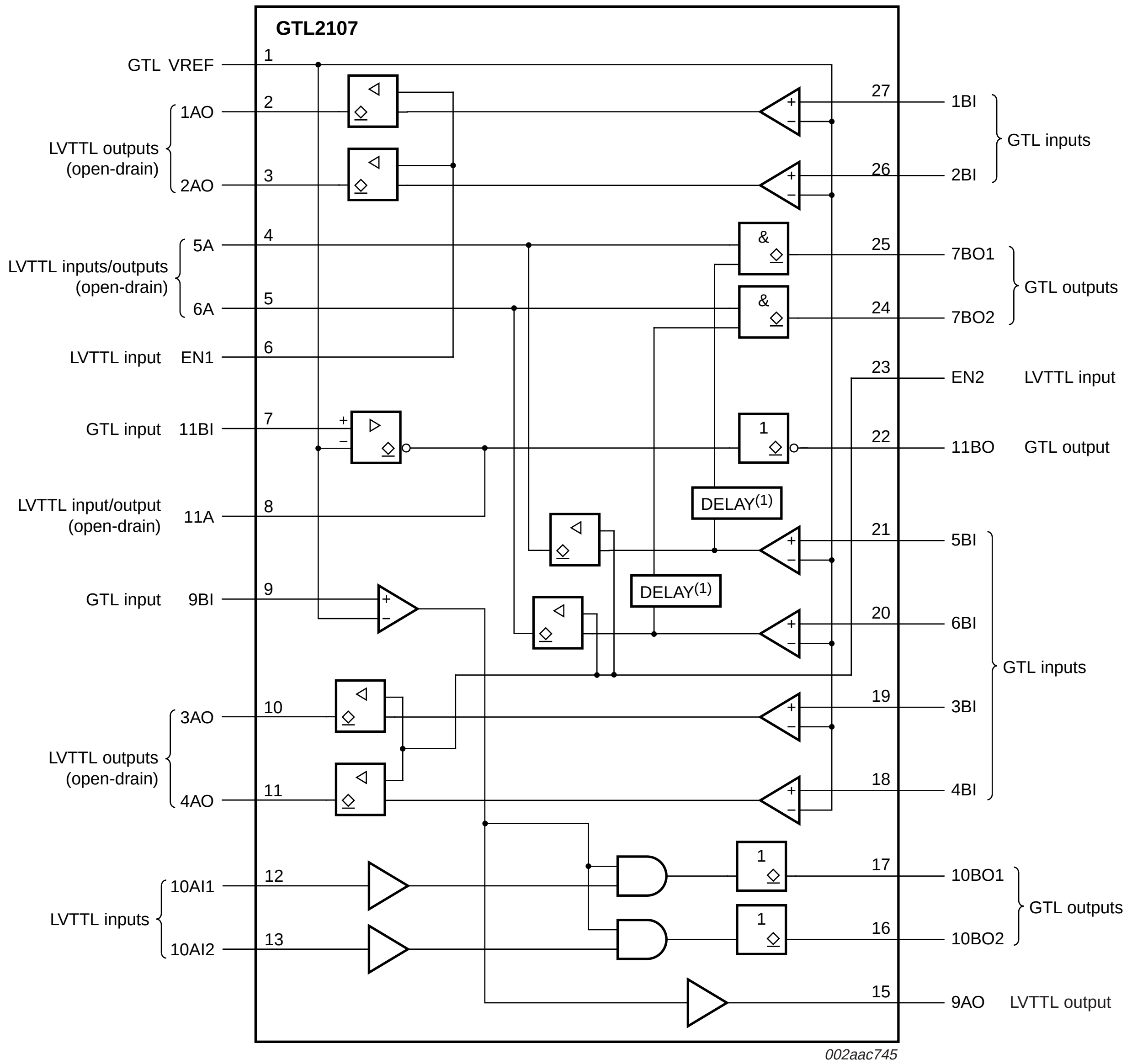
4. Ordering information

Table 2. Ordering information

T_{amb} = −40 °C to +85 °C

Type number	Topside mark	Package		
		Name	Description	Version
GTL2107PW	GTL2107	TSSOP28	plastic thin shrink small outline package; 28 leads; body width 4.4 mm	SOT361-1

5. Functional diagram



(1) The enable on 7BO1/7BO2 include a delay that prevents the transient condition (where 5BI/6BI go from LOW to HIGH, and the LOW to HIGH on 5A/6A lags up to 100 ns) from causing a LOW glitch on the 7BO1/7BO2 outputs.

Fig 1. Logic diagram of GTL2107

6. Pinning information

6.1 Pinning

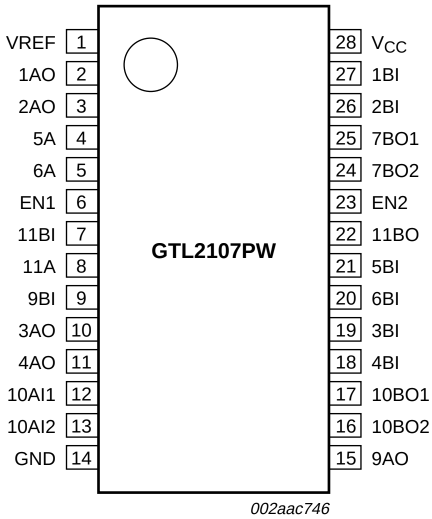


Fig 2. Pin configuration for TSSOP28

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
VREF	1	GTL reference voltage
1AO	2	data output (LVTTL), open-drain
2AO	3	data output (LVTTL), open-drain
5A	4	data input/output (LVTTL), open-drain
6A	5	data input/output (LVTTL), open-drain
EN1	6	enable input (LVTTL)
11BI	7	data input (GTL)
11A	8	data input/output (LVTTL), open-drain
9BI	9	data input (GTL)
3AO	10	data output (LVTTL), open-drain
4AO	11	data output (LVTTL), open-drain
10AI1	12	data input (LVTTL)
10AI2	13	data input (LVTTL)
GND	14	ground (0 V)
9AO	15	data output (LVTTL), push-pull
10BO2	16	data output (GTL)
10BO1	17	data output (GTL)
4BI	18	data input (GTL)
3BI	19	data input (GTL)

Table 3. Pin description *…continued*

Symbol	Pin	Description
6BI	20	data input (GTL)
5BI	21	data input (GTL)
11BO	22	data output (GTL)
EN2	23	enable input (LVTTL)
7BO2	24	data output (GTL)
7BO1	25	data output (GTL)
2BI	26	data input (GTL)
1BI	27	data input (GTL)
V_{CC}	28	positive supply voltage

7. Functional description

Refer to Figure 1 “Logic diagram of GTL2107”.

7.1 Function tables

Table 4. Power supervisor power good control

H = HIGH voltage level; L = LOW voltage level; X = Don’t care.

Inputs		Output
EN1	**1BI/2BI**	**1AO/2AO (open-drain)**
H	L	L
H	H	H
L	X	H

Table 5. Power supervisor power good control

H = HIGH voltage level; L = LOW voltage level; X = Don’t care.

Inputs		Output
EN2	**3BI/4BI**	**3AO/4AO (open-drain)**
H	L	L
H	H	H
L	X	H

Table 6. Southbridge SMI_L control

H = HIGH voltage level; L = LOW voltage level.

Input	Output
9BI	**9AO (push-pull)**
L	L
H	H

Table 7. CPU SMI_L control

H = HIGH voltage level; L = LOW voltage level.

Inputs		Output
10AI1/10AI2	9BI	10BO1/10BO2
L	L	L
L	H	L
H	L	L
H	H	H

Table 8. PROCHOT L control

H = HIGH voltage level; L = LOW voltage level.

Inputs		Input/output	Output
EN2	5BI/6BI	5A/6A (open-drain)	7BO1/7BO2
H	L	L	H[1]
H	H	L[2]	L
H	H	H	H
L	H	L[2]	L
L	H	H	H
L	L	H	H
L	L	L[2]	H

[1] The enable on 7BO1/7BO2 includes a delay that prevents the transient condition (where 5BI/6BI goes from LOW to HIGH, and the LOW to HIGH on 5A/6A lags up to 100 ns) from causing a low glitch on the 7BO1/7BO2 outputs.

[2] Open-drain input/output terminal is driven to logic LOW state by an external driver.

Table 9. Southbridge NMI control

H = HIGH voltage level; L = LOW voltage level.

Input	Input/output	Output
11BI	11A (open-drain)	11BO
L	H	L
L	L[1]	H
H	L	H

[1] Open-drain input/output terminal is driven to logic LOW state by an external driver.

8. Application design-in information

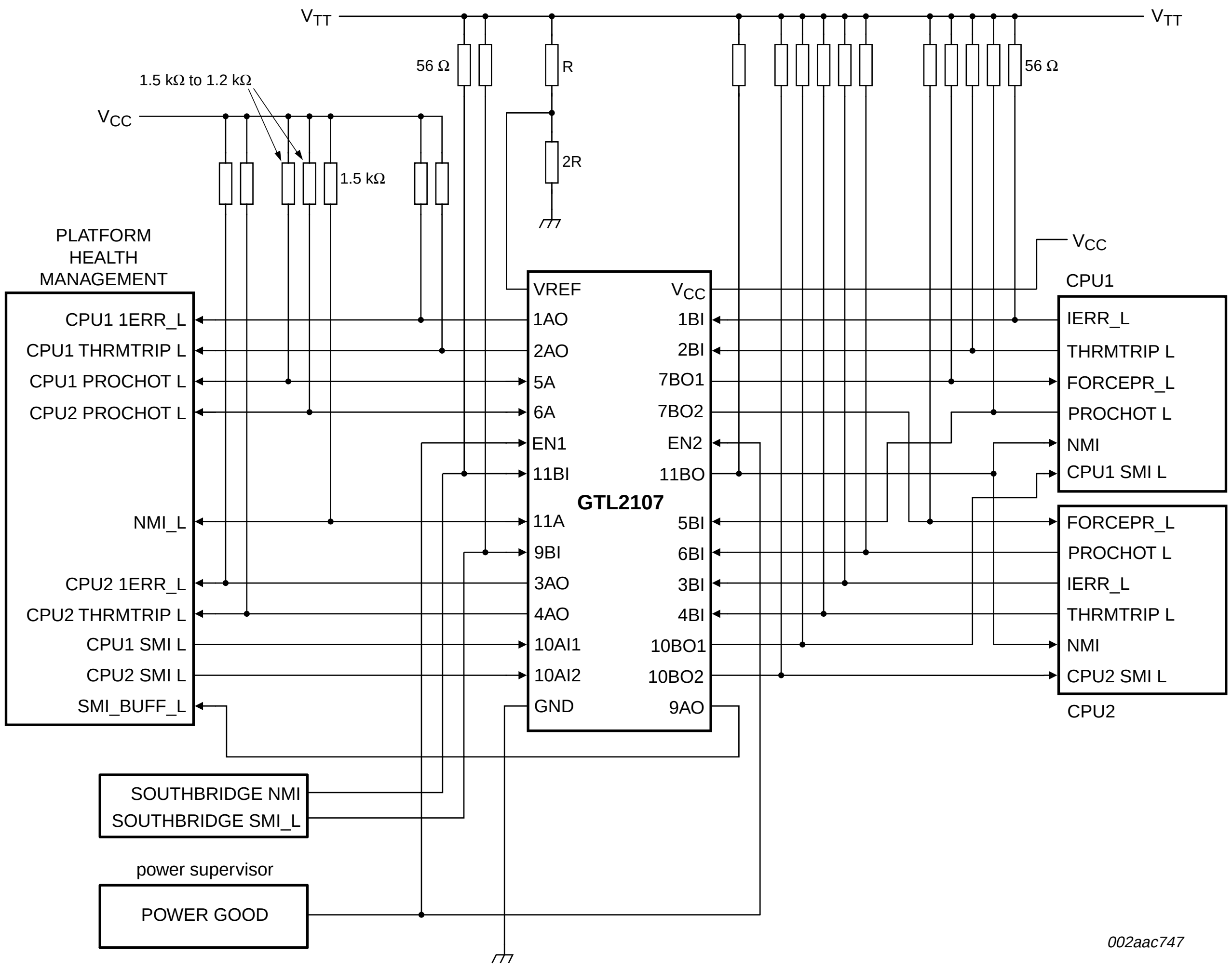


Fig 3. Typical application

9. Limiting values

Table 10. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).
Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.5	+4.6	V
I_{IK}	input clamping current	$V_I < 0$ V	-	–50	mA
V_I	input voltage	A port (LVTTL)	–0.5[1]	+4.6	V
		B port (GTL)	–0.5[1]	+4.6	V
I_{OK}	output clamping current	$V_O < 0$ V	-	–50	mA
V_O	output voltage	output in OFF or HIGH state; A port	–0.5[1]	+4.6	V
		output in OFF or HIGH state; B port	–0.5[1]	+4.6	V
I_{OL}	LOW-level output current[2]	A port	-	32	mA
		B port	-	30	mA
I_{OH}	HIGH-level output current[3]	A port	-	–32	mA
T_{stg}	storage temperature		–60	+150	°C
$T_{j(max)}$	maximum junction temperature	[4]	-	+125	°C

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] Current into any output in the LOW state.

[3] Current into any output in the HIGH state.

[4] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

10. Recommended operating conditions

Table 11. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		3.0	3.3	3.6	V
V_{TT}	termination voltage	GTL–	0.85	0.9	0.95	V
		GTL	1.14	1.2	1.26	V
		GTL+	1.35	1.5	1.65	V
V_{ref}	reference voltage	overall	0.5	$\frac{2}{3}V_{TT}$	1.8	V
		GTL–	0.5	0.6	0.63	V
		GTL	0.76	0.8	0.84	V
		GTL+	0.87	1	1.1	V
V_I	input voltage	A port	0	3.3	3.6	V
		B port	0	V_{TT}	3.6	V
V_{IH}	HIGH-level input voltage	A port and ENn	2	-	-	V
		B port	$V_{ref} + 0.050$	-	-	V
V_{IL}	LOW-level input voltage	A port and ENn	-	-	0.8	V
		B port	-	-	$V_{ref} - 0.050$	V
I_{OH}	HIGH-level output current	A port	-	-	–16	mA

Table 11. Operating conditions *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{OL}	LOW-level output current	A port	-	-	16	mA
		B port	-	-	15	mA
T_{amb}	ambient temperature	operating in free-air	–40	-	+85	°C

11. Static characteristics

Table 12. Static characteristics

Recommended operating conditions; voltages are referenced to GND (ground = 0 V). T_{amb} = –40 °C to +85 °C

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{OH}	HIGH-level output voltage	9AO; V_{CC} = 3.0 V to 3.6 V; I_{OH} = –100 μA	[2]	V_{CC} – 0.2	3.0	-	V
		9AO; V_{CC} = 3.0 V; I_{OH} = –16 mA	[2]	2.1	2.3	-	V
V_{OL}	LOW-level output voltage	A port; V_{CC} = 3.0 V; I_{OL} = 4 mA	[2]	-	0.15	0.4	V
		A port; V_{CC} = 3.0 V; I_{OL} = 8 mA	[2]	-	0.3	0.55	V
		A port; V_{CC} = 3.0 V; I_{OL} = 16 mA	[2]	-	0.6	0.8	V
		B port; V_{CC} = 3.0 V; I_{OL} = 15 mA	[2]	-	0.13	0.4	V
I_{OH}	HIGH-level output current	open-drain outputs; A port other than 9AO; V_O = V_{CC}; V_{CC} = 3.6 V		-	-	±1	μA
I_I	input current	A port; V_{CC} = 3.6 V; V_I = V_{CC}		-	-	±1	μA
		A port; V_{CC} = 3.6 V; V_I = 0 V		-	-	±1	μA
		B port; V_{CC} = 3.6 V; V_I = V_{TT} or GND		-	-	±1	μA
I_{CC}	supply current	A or B port; V_{CC} = 3.6 V; V_I = V_{CC} or GND; I_O = 0 mA		-	8	12	mA
ΔI_{CC}[3]	additional supply current	per input; A port or control inputs; V_{CC} = 3.6 V; V_I = V_{CC} – 0.6 V		-	-	500	μA
C_{io}	input/output capacitance	A port; V_O = 3.0 V or 0 V		-	3.0	4.0	pF
		B port; V_O = V_{TT} or 0 V		-	2.0	3.0	pF

[1] All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

[2] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[3] This is the increase in supply current for each input that is at the specified LVTTL voltage level rather than V_{CC} or GND.

12. Dynamic characteristics

Table 13. Dynamic characteristics

V_{CC} = 3.3 V ± 0.3 V

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{ref} = 0.73 V; V_{TT} = 1.1 V							
t_{PLH}	LOW-to-HIGH propagation delay	nA to nBI; see Figure 4		1	4	8	ns
		9BI to 9AO; see Figure 5		2	5.5	10	ns
		nBI to nA or nAO (open-drain outputs); see Figure 14		2	13	18	ns
		9BI to 10BOn		2	6	11	ns
		11A to 11BO; see Figure 10		1	4	8	ns
		11BI to 11A; see Figure 9		2	7.5	11	ns
		11BI to 11BO		2	8	13	ns
		5BI to 7BO1 or 6BI to 7BO2; see Figure 7		4	7	11	ns
t_{PHL}	HIGH-to-LOW propagation delay	nA to nBI; see Figure 4		2	5.5	10	ns
		9BI to 9AO; see Figure 5		2	5.5	10	ns
		nBI to nA or nAO (open-drain outputs); see Figure 14		2	4	10	ns
		9BI to 10BOn		2	6	11	ns
		11A to 11BO; see Figure 10		1	5.5	10	ns
		11BI to 11A; see Figure 9		2	8.5	13	ns
		11BI to 11BO	[2]	2	14	21	ns
		5BI to 7BO1 or 6BI to 7BO2; see Figure 7		100	205	350	ns
t_{PLZ}	LOW to OFF-state propagation delay	EN1 to nAO or EN2 to nAO; see Figure 8		1	3	7	ns
		EN1 to 5A (I/O) or EN2 to 6A (I/O); see Figure 8		1	3	7	ns
t_{PZL}	OFF-state to LOW propagation delay	EN1 to nAO or EN2 to nAO; see Figure 8		1	3	7	ns
		EN1 to 5A (I/O) or EN2 to 6A (I/O); see Figure 8		1	3	7	ns
t_{PHZ}	HIGH to OFF-state propagation delay	EN2 to 9AO; see Figure 11		2	5	10	ns
t_{PZH}	OFF-state to HIGH propagation delay	EN2 to 9AO; see Figure 11		1	4	10	ns

Table 13. Dynamic characteristics *...continued*

V_{CC} = 3.3 V ± 0.3 V

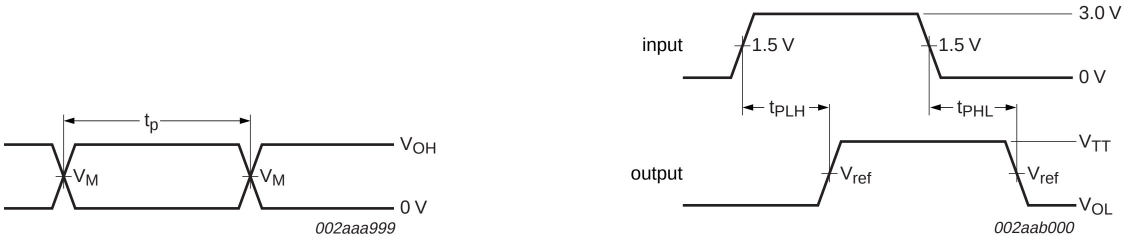
Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{ref} = 0.76 V; V_{TT} = 1.2 V							
t_{PLH}	LOW-to-HIGH propagation delay	nA to nBI; see Figure 4		1	4	8	ns
		9BI to 9AO; see Figure 5		2	5.5	10	ns
		nBI to nA or nAO (open-drain outputs); see Figure 14		2	13	18	ns
		9BI to 10BOn		2	6	11	ns
		11A to 11BO; see Figure 10		1	4	8	ns
		11BI to 11A; see Figure 9		2	7.5	11	ns
		11BI to 11BO		2	8	13	ns
		5BI to 7BO1 or 6BI to 7BO2; see Figure 7		4	7	11	ns
t_{PHL}	HIGH-to-LOW propagation delay	nA to nBI; see Figure 4		2	5.5	10	ns
		9BI to 9AO; see Figure 5		2	5.5	10	ns
		nBI to nA or nAO (open-drain outputs); see Figure 14		2	4	10	ns
		9BI to 10BOn		2	6	11	ns
		11A to 11BO; see Figure 10		1	5.5	10	ns
		11BI to 11A; see Figure 9		2	8.5	13	ns
		11BI to 11BO	[2]	2	14	21	ns
		5BI to 7BO1 or 6BI to 7BO2; see Figure 7		100	205	350	ns
t_{PLZ}	LOW to OFF-state propagation delay	EN1 to nAO or EN2 to nAO; see Figure 8		1	3	7	ns
		EN1 to 5A (I/O) or EN2 to 6A (I/O); see Figure 8		1	3	7	ns
t_{PZL}	OFF-state to LOW propagation delay	EN1 to nAO or EN2 to nAO; see Figure 8		1	3	7	ns
		EN1 to 5A (I/O) or EN2 to 6A (I/O); see Figure 8		1	3	7	ns
t_{PHZ}	HIGH to OFF-state propagation delay	EN2 to 9AO; see Figure 11		2	5	10	ns
t_{PZH}	OFF-state to HIGH propagation delay	EN2 to 9AO; see Figure 11		2	4	10	ns

[1] All typical values are at V_{CC} = 3.3 V and T_{amb} = 25 °C.

[2] Includes ~7.6 ns RC rise time of test load pull-up on 11A, 1.5 kΩ pull-up and 21 pF load on 11A has about 23 ns RC rise time.

12.1 Waveforms

V_M = 1.5 V at $V_{CC} \geq 3.0$ V for A ports; $V_M = V_{ref}$ for B ports.



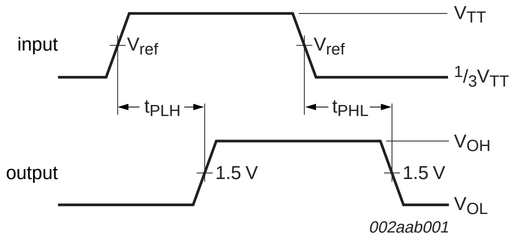
V_M = 1.5 V for A port and V_{ref} for B port

a. Pulse duration

A port to B port

b. Propagation delay times

Fig 4. Voltage waveforms



PRR ≤ 10 MHz; $Z_o = 50\ \Omega$; $t_r \leq 2.5$ ns; $t_f \leq 2.5$ ns

Fig 5. Propagation delay, 9BI to 9AO

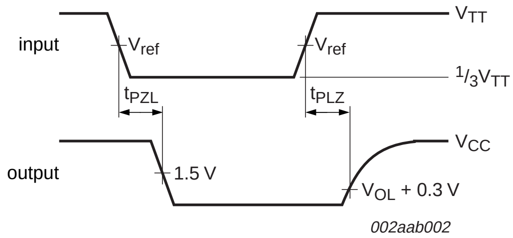


Fig 6. nBI to nA (I/O) or nBI to nAO open-drain outputs

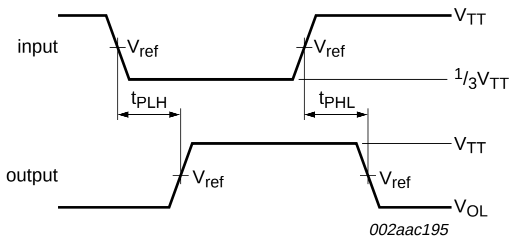


Fig 7. 5BI to 7BO1 or 6BI to 7BO2

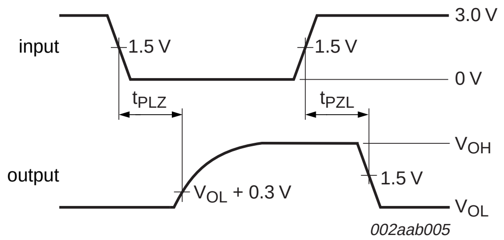


Fig 8. EN1 to 5A (I/O) or EN2 to 6A (I/O) or EN1 to nAO or EN2 to nAO

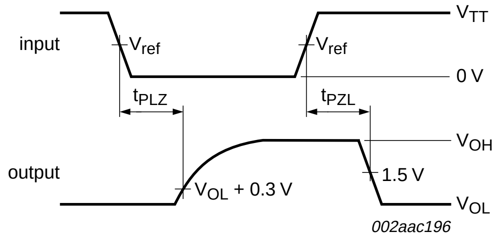


Fig 9. 11BI to 11A

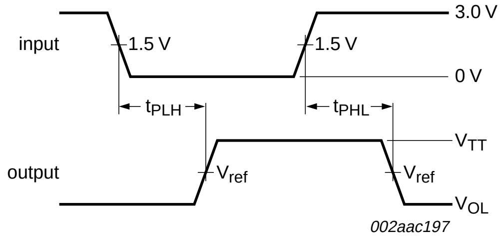


Fig 10. 11A to 11BO

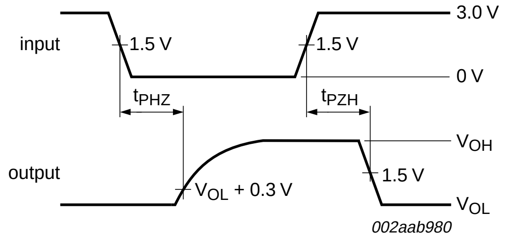


Fig 11. EN2 to 9AO

13. Test information

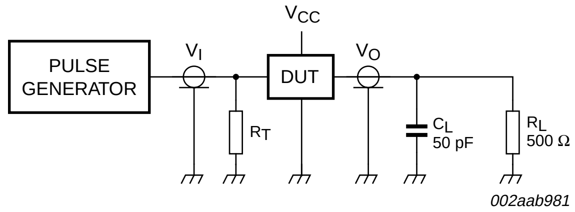


Fig 12. Load circuit for A outputs (9AO)

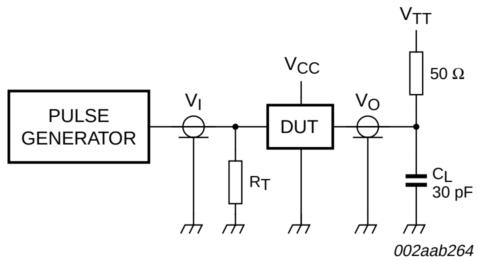


Fig 13. Load circuit for B outputs

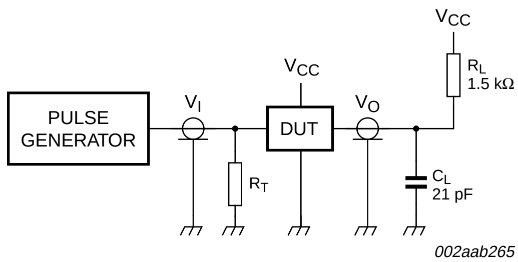


Fig 14. Load circuit for open-drain LVTTL I/O and open-drain outputs

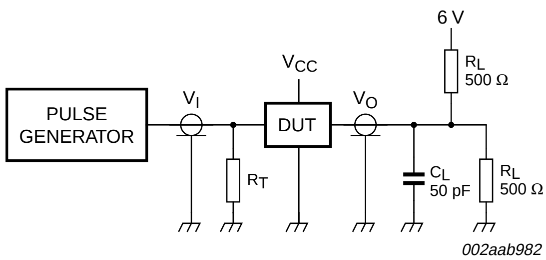


Fig 15. Load circuit for 9AO OFF-state to LOW and LOW to OFF-state

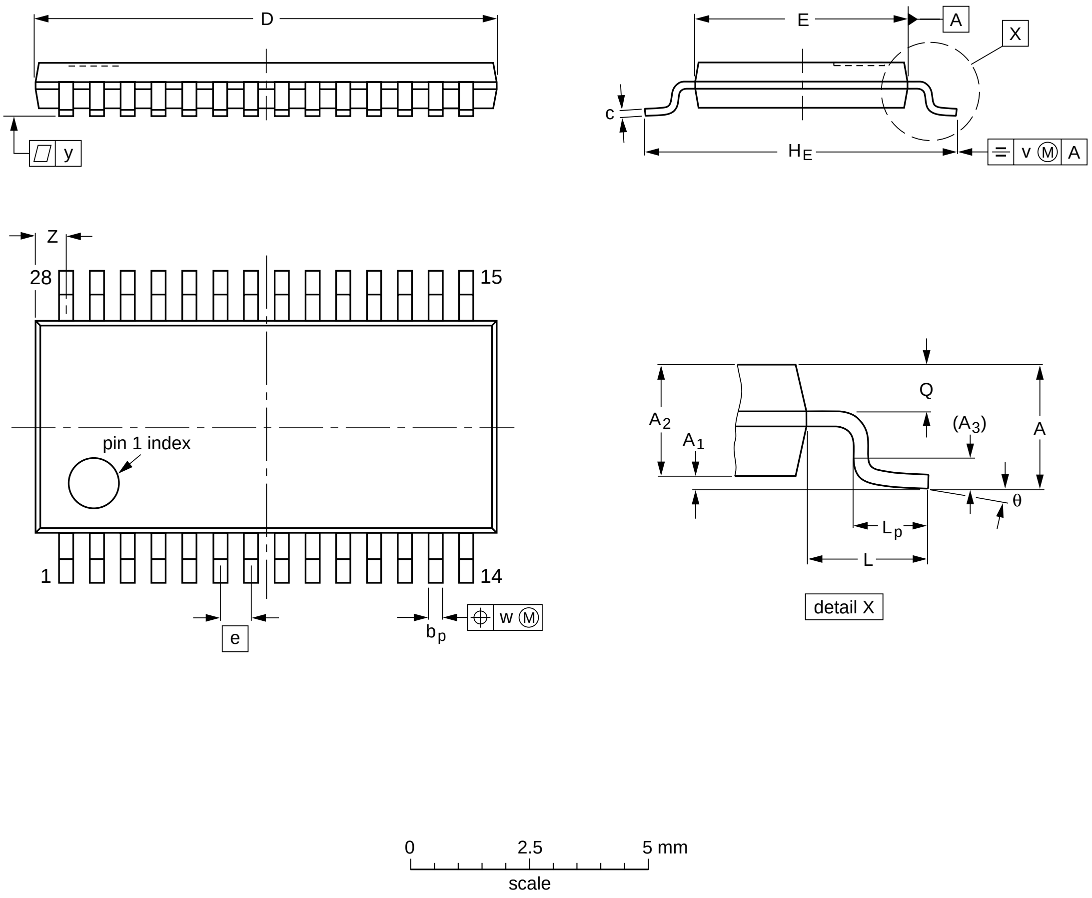
R_L — Load resistor

C_L — Load capacitance; includes jig and probe capacitance

R_T — Termination resistance; should be equal to Z_o of pulse generators.

14. Package outline

TSSOP28: plastic thin shrink small outline package; 28 leads; body width 4.4 mm **SOT361-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	9.8 9.6	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.8 0.5	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT361-1		MO-153				~~99-12-27~~ 03-02-19

Fig 16. Package outline SOT361-1 (TSSOP28)

15. Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 “Surface mount reflow soldering description”*.

15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus PbSn soldering

15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 17) than a PbSn process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 14 and 15

Table 14. SnPb eutectic process (from J-STD-020C)

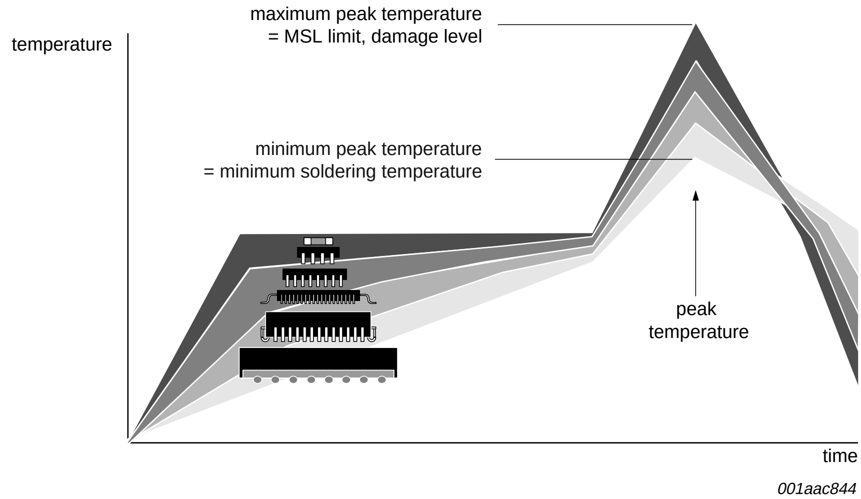
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 15. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 17.



MSL: Moisture Sensitivity Level

Fig 17. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 “Surface mount reflow soldering description”*.

16. Abbreviations

Table 16. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
DUT	Device Under Test
ESD	ElectroStatic Discharge
GTL	Gunning Transceiver Logic
HBM	Human Body Model
LVTTL	Low Voltage Transistor-Transistor Logic
MM	Machine Model
PRR	Pulse Rate Repetition
TTL	Transistor-Transistor Logic
VRD	Voltage Regulator Down

17. Revision history

Table 17. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
GTL2107_4	20070706	Product data sheet	-	GTL2107_3
Modifications:	• Table 1 "Quick reference data" and Table 12 "Static characteristics": – C_{io}, input/output capacitance; A port: Typ value changed from 2.5 pF to 3.0 pF – C_{io}, input/output capacitance; A port: Max value changed from 3.5 pF to 4.0 pF – C_{io}, input/output capacitance; B port: Typ value changed from 1.5 pF to 2.0 pF – C_{io}, input/output capacitance; B port: Max value changed from 2.5 pF to 3.0 pF			
GTL2107_3	20070129	Objective data sheet	-	GTL2008_GTL2107_2
GTL2008_GTL2107_2	20060926	Product data sheet	-	GTL2008_1
GTL2008_1	20060502	Product data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

18.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

18.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of a NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer’s own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

18.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

19. Contact information

For additional information, please visit: **http://www.nxp.com**

For sales office addresses, send an email to: **salesaddresses@nxp.com**

20. Contents

Date of release: 6 July 2007
Document identifier: GTL2107_4